In the Specification

The paragraph beginning on page 14, line 9 is amended as follows:

As described in FIG. 5, X is calculated by ~~comparing~~ calculating unit 410. The Io code is set based on the value of X. For example, Io is zero when X is less than or equal to B/2 and Io is one when X is greater than B/2 where B is the number of bits of DO (DOp or Dout). In FIG. 6, B=8. Thus, in row 1, Io is one (1) because X is greater than four (4). In row 6, Io is zero because X is less than four.

The paragraph beginning on page 21, line 12 is amended as follows:

FIG. 18 is a circuit diagram of a calibrating circuit according to an embodiment of the invention. Calibrating circuit 1800 may be used as calibrating circuit [[314]] 316 of FIG. 3. In FIG. 18, calibrating circuit 1800 receives a number of timing calibrating codes CA-0 through CA-M. A combination of the CA-0 through CA-M codes on auxiliary lines 1811 represents a timing delay. In some embodiments, the CA-0 through CA-M codes is provided to memory device 100 (FIG. 1) by an external device such as a memory controller or a processors.